John L. Cooper (State Bar No. 050324)
jcooper@fbm.com
Stephanie Powers Skaff (State Bar No. 183119)
sskaff@fbm.com
Eugene Y. Mar (State Bar No. 227071)
emar@fbm.com
Farella Braun & Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
Telephone: (415) 954-4400
Facsimile: (415) 954-4480

Attorneys for Defendants
TECHNOLOGY PROPERTIES LTD. AND
ALLIACENSE LTD.

Charles T. Hoge, Esq. (State Bar No. 110696)
choge@knlh.com
Kirby Noonan Lance & Hoge
35 Tenth Avenue
San Diego, CA 92101
Telephone: (619) 231-8666
Facsimile: (619) 231-9593

Attorneys for Defendant
PATRIOT SCIENTIFIC CORPORATION

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00877 JR/HRL

CORRECTED*

DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF
(Patent L.R. 4-5(a))

[RELATED CASES]

Date: TBD
Time: TBD
Dept: Courtroom 3, 5th Floor
Before: Hon. Jeremy Fogel

* Administrative error on caption page and signature block are corrected

HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 JF/HRL
BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORP., ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-05398 JF/HRL

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

TABLE OF CONTENTS

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

TABLE OF AUTHORITIES

FEDERAL CASES

FEDERAL STATUTES

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

I. INTRODUCTION

Defendants Technology Properties Limited ("TPL") and Patriot Scientific Corp. (collectively "Defendants")[1] own the patents in this litigation, which claim novel architectures and clocking mechanisms critical to the efficient and high-speed performance of today's microprocessors. Charles Moore ("Moore") and Russell Fish ("Fish") are the co-inventors of these pioneer patents. Between late 1988 and 1989, Moore and Fish designed a 32-bit microprocessor, named "ShBoom."[2] On August 3, 1989, Moore and Fish filed a comprehensive microprocessor patent application. Seven patents, including the patents-in-suit, ultimately issued. In the intervening years, over 80 global electronics firms (including Intel, Sony, HP and others) have licensed the patents from TPL, and the patents have withstood over fifteen reexaminations.

TPL and its affiliated companies specialize in the development, commercialization and management of intellectual property assets, including the patents-in-suit. On the product development side, utilizing licensing proceeds, TPL develops microprocessors using the claimed inventions in general applications such as USB control, and special applications such as hearing aids. Patriot is the assignee of Fish's rights in and to the patents-in-suit. Historically, Patriot developed hybrid RISC-stack technology, which resulted in smaller, lower power, less expensive system-on-chip designs. Today Patriot markets and enables innovative proprietary technologies.

II. THE PATENTED TECHNOLOGY

The four patents-in-suit share the same specification, albeit with slight differences in pagination. The patent portfolio has been the subject of a combined total of at least 15 ex parte reexamination proceedings before the U.S. Patent and Trademark Office ("USPTO"). The first

[1] The plaintiffs from all three related actions, Acer Inc., Acer America Corp., and Gateway, Inc. (collectively "Acer"), HTC Corporation and HTC America Inc. (collectively "HTC"), and Barco, N.V. ("Barco") (collectively "Plaintiffs"), coordinated their proposed claim constructions, as shown in the Joint Claims Construction Statement, filed October 29, 2010 ("JCCS"). Plaintiffs and Defendants agreed on the construction of 33 claim terms, and this brief addresses the remaining 30 disputed terms across the four patents in suit. All four patents are at issue in the *Acer v. TPL* and *HTC v. TPL* actions, while only three of the four are at issue in *Barco v. TPL*. The Patent Local Rule requiring parties to identify the most significant claim terms applies only to the *Barco* action. This brief generally addresses the most significant and potentially case dispositive claim terms first and follows with the remaining miscellaneous terms.

[2] ShBoom operated in a computer language known as "Forth" that was developed by Moore. Moore received a presidential award for his accomplishments in developing Forth.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

'336 patent reexamination certificate issued on December 15, 2009; the second reexamination certificate issued on November 3, 2010. Collectively, the '336 patent overcame 607 references that were raised against it in reexamination. Similarly, the USPTO recently issued a Notice of Intent to Reissue Certificate for the '890 patent over 614 cited references. To date, 382 references have been raised against the '148 patent, and 846 references have been raised against the '749 patent; both are still in reexamination.

A. Background of the Technology of the '336 Patent

Microprocessors are complex machines, with millions of individual parts whose operation requires coordination, both internally and with external components, for the chip to function properly. This coordination is performed by clock signals. U.S. Patent No. 5,809,336 ('the '336 patent"), entitled "High Performance Microprocessor Having Variable Speed System Clock," (Declaration of Eugene Mar in Support of Defendants' Opening Claim Construction Brief (Mar Dec.), Ex. A) teaches the use of two independent clocks in a microprocessor system – an on-chip first clock to time the CPU, and a second independent clock to time the input/output (I/O) interface. This innovation was widely adopted by the industry and became fundamental to the increased speed and efficiency of modern microprocessors. Decoupling the system clock from the I/O clock allowed the clocks to run independently (or "asynchronously"), freeing the system clock, and thus the CPU, to run faster when needed (or more slowly to conserve power). This decoupling had the added benefit of reducing the sensitivity of the system as whole to temperature, voltage and manufacturing variations, since the on-chip first clock and the CPU could vary together in response to such variations, with minimal impact on the I/O interface due to the second clock domain.

B. Background of the Technology of the '148 Patent

U.S. Patent No. 6,598,148 ('the '148 patent") also entitled "High Performance Microprocessor Having Variable Speed System Clock," (Mar Dec., Ex. I) teaches a microprocessor that combines the on-chip first clock of the '336 patent with the use of more than 50% of the surface area of the integrated circuit for memory. This substantial increase in on-chip memory supports faster microprocessors, and potentially cheaper systems.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

C. Background of the Technology of the '890 Patent

U.S. Patent No. 5,330,890 ("the '890 patent"), entitled "High Performance, Low Cost Microprocessor Architecture," (Mar Dec., Ex. K) teaches a dual stack architecture and the use of stack pointers that that can reference memory in any location to provide more architectural flexibility and faster access to data elements. Combining this with other features, such as a memory controller and direct memory access, the '890 patent allows the CPU to off-load memory transfer of data to achieve further efficiencies and higher performance.

D. Background of the Technology of the '749 Patent

Microprocessors operate instructions that are usually stored in a memory that is slower than the CPU. U.S. Patent No. 5,440,749 ("the '749 patent,"), entitled "High Performance, Low Cost Microprocessor Architecture,"(Mar Dec., Ex. M) teaches a processor that fetches multiple instructions at a time, and then supplies them to the CPU in parallel (at the same time) in a single memory cycle. Since memory is generally slower than the CPU, being able to fetch and supply more than one instruction at a time increases the amount of instructions the CPU can receive in a given time, and thus increases instruction bandwidth.

The '749 combines this technology with the last-in first-out data organization also called a "pushdown stack." A stack is an efficient way of organizing data in computer memory that uses a last-in first-out data structure, and an intuitive way of organizing data for a processor to perform arithmetic functions.

III. LEGAL STANDARD FOR CLAIM CONSTRUCTION

The proper construction of claims is a legal determination. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (*en banc*), *aff'd*, 517 U.S. 370 (1996). To ascertain the meaning of terms used in the patent claims, courts first consider a patent's intrinsic evidence, which includes the claims themselves, the specification, and the prosecution history. *Markman*, 52 F.3d at 979; *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1315-17 (Fed. Cir. 2005). Courts may also rely on extrinsic evidence such as dictionary definitions, expert opinion, and the prior art. *Markman*, 52 F.3d at 980-81. In construing claims, it is "unjust to the public, as well as an evasion of the law, to construe it in a manner different from the plain import of its

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

terms." *Phillips*, 415 F.3d at 1312 (citation omitted). This is because "[i]t is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips*, 415 F.3d at 1312 (*quoting Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)).

The words of a claim are generally given their ordinary and customary meaning as understood by a person of ordinary skill in the art at the time of the invention. Although the specification may describe specific embodiments, the claims are not limited to those embodiments. *Kara Tech., Inc. v. Stamps.com Inc.*, 582 F.3d 1341, 1347-48 (Fed. Cir. 2009).

IV. CONSTRUCTION OF DISPUTED CLAIM TERMS.

The parties dispute the proper construction of 30 claim terms from the asserted patents. In nearly every instance, the dispute centers on Plaintiffs' attempts to import limitations on the claim that would either limit the claims to a preferred embodiment or exclude a preferred embodiment. The disputed terms, their proposed constructions, and their support, are specified in the parties' Patent Local Rule 4-3 filing of the Joint Claims Construction Statement, Exhibits B-D, (Dkt. 203 (Acer)) ("JCCS").

A. "Push Down Stack" and Related Terms

The parties dispute the proper construction of the term "push down stack" and related terms concerning how push down stacks connect to arithmetic logic units ("ALU").

1. The Patents Disclose a Variety of "Push Down Stacks." (JCCS Row 2) (*passim* across asserted patents and claims)

Plaintiffs' Construction	TPL's Construction
a group of data storage elements organized **from top to bottom** to provide last-in first-out access to **stored** items, **wherein any previously stored items propagate towards the bottom by one data storage element while a new item is stored in the top data storage element**	Data storage elements organized to provide last-in first-out access to items

The parties agree that a "push down stack" — also referred to as a "stack" — consists of data storage elements organized to provide last-in, first-out ("LIFO") access to items. *See, e.g.*, '890 Reexam Hist.; Mar Dec., Ex. L at TPL-VO004406 (citing extrinsic evidence "stack is

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

sometimes referred to as a last-in-first-out or LIFO data structure"); *see also*, The Computer Glossary, 651, Mar Dec., Ex. S. This last-in-first-out property is also expressed in terms of "pushing" and "popping." "The last item, or address, placed (pushed) onto the stack is the first item removed (popped) from the stack." *Id*. The patent prescribes that:

> [f]or math and logic operations, the microprocessor 50 exploits the inherent advantage of a stack by designating the source operand(s) as the top stack item and the next stack item. The math or logic operation is performed, the operands are ***popped*** from the stack, and the result is ***pushed*** back on the stack. (emphasis added).

'890 patent, 24:9-15; Mar Dec., Ex. K.

Although the parties agree that a push down stack is a data storage element organized on a LIFO basis, Plaintiffs attempt to impose extraneous limitations on the structure of push down stacks, requiring them to have "a group of data storage elements organized from top to bottom," and for items to "propagate towards the bottom by one data storage element." These limitations are not required by the ordinary meaning of the term "stack" and the patents do not depart from or disclaim the ordinary meaning so as to limit stacks to data storage elements in a top down relationship. *Phillips*, 415 F.3d at 1316. Plaintiffs' mischief was revealed by their expert Dr. Wolfe, who testified the patents exclusively disclose a "stack processor" that utilizes "hardware stacks":

> Q: When you use the term "stack processor," what do you mean by that phrase?
>
> A: Loosely, it's used to describe processors in which the CPU performs its operations on a hardware stack structure. It obtains the operands for its instructions from a hardware stack rather than from general-purpose registers or special dedicated operand registers.
>
> Instead, it stores all of its inputs to operations on a particular structure called a hardware stack and uses those both to supply the operands for calculations and to store the results of calculations.
>
> ****
>
> Q: How do you implement a hardware stack?
>
> A: Generally the way you implement a hardware stack is, you have some storage structure, usually registers and it operates in such a way that when you add something to the top of the stack, the position of every other piece of data gets moved down; and when you remove something from the top of the stack, the position of every other piece of data gets moved up.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

Wolfe Dep. 26:14-27:10, 29:13-21; Mar Dec., Ex. V. While Plaintiffs would like to limit the stacks of the specification to "hardware stacks," and their claim construction is carefully calibrated to such an arrangement, the patents are not so limiting.

The patents disclose a variety of stacks. Yet, none of the embodiments is called a "hardware stack," and none discusses how pieces of data are ***physically*** arranged or ***physically propagate*** from element-to-element upon a push or a pop. To the contrary, some use general purpose memory such as RAM to store data items, and in several the microprocessor uses stack pointers to track the contents of and operate the stacks. Figure 2 discloses a push down stack (74) connected to top and next item registers (76 and 78), which provide inputs to, and receive output from, the ALU. '890 patent, 6:21-27; Mar Dec., Ex. K. The specification does not state that 74 is a "hardware stack" or that data items must physically propagate from element to element. Figures 2 and 13 both show the use of stack pointers to track and operate the stack. Having pointers "point to" the location of the data storage elements would be unnecessary if the data was always physically stacked in a single location and propagated from element-to-element. '749 patent, 19:35-38; Mar Dec. Ex. M. The return push down stack is also disclosed as using addressable registers. *Id*., 31:46-57.

Figure 21 drives this point home, showing a novel triple cache stack architecture utilizing ***on-chip*** and ***off-chip*** memory including RAM to store stack elements. *Id*., 19:6-43. RAM is by definition "random access memory," so it has no requirement that data must "propagate" in any particular way through RAM. The elements of this stack are organized by the microprocessor using multiple ***stack pointers***.[3] *Id*., 19:20-23; 35-38. The disparate on-chip and off-chip memory locations are not arranged from "top to bottom."[4] Plaintiffs' claim construction would read out this embodiment, and is therefore improper. *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1377 (Fed. Cir. 2005) (reading out a preferred embodiment "would rarely if ever be correct.").

[3] *See*, The Computer Dictionary (stack pointer: "A register that contains the current address of the top element of the stack."); Mar Dec., Ex. T.

[4] Extrinsic evidence confirms that the ordinary meaning of "stack" is not limited to the type of hardware register Plaintiffs' construction contemplates. *See, e.g.*, The Computer Glossary (" a set of hardware registers ***or*** a reserved amount of main memory . . .") Mar Dec., Ex. S.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

2. Plaintiffs' attempt to impose limitations on the connection of the ALU and first push down stack excludes preferred embodiments.

The parties' competing constructions for claims reciting how a push down stack connects to the ALU are exemplified here:

- "Push down stack connected to said ALU" (JCCS Row 1) ('749 patent, claims 1 and 9)

Plaintiffs' Construction	TPL's Construction
A push down stack comprising a top item register and a next item register, both **directly coupled** to the ALU **such that source and destination addresses are not used**	Ordinary meaning unless already defined – "push down stack," "connected to," "ALU"

The same dispute occurs in JCCS Rows 3, 8, 9, 15, 16. TPL proposes that claim terms covering how push down stacks (and their top and next registers) are "connected to" the ALU should be construed according to their ordinary meaning except for sub-terms elsewhere construed, such as "push down stack," "connected to" and "ALU." Plaintiffs import the narrowing limitation that the stack be "directly coupled to the ALU such that source and destination addresses are not used," which is incorrect and excludes preferred embodiments.

a. The Plain Language of the Terms Requires Only That the ALU Be "Connected To" the Stack

The plain language of these claim terms recites that a push down stack is connected to an ALU. Claim terms are typically given their plain and ordinary meaning and here there was no disavowal, so these terms should be given their full scope. *Kara Tech., Inc.*, 582 F.3d at 1347-48. A connection to carry signals is all that is required. See below IV(D) ("connected to").

b. The Specification Contemplates That a Stack Can Be Used With Addresses While Maintaining the Speed Benefits of the Invention's Multiple Instruction Fetch

One of the points of novelty of the patents, particularly the '749 patent, was to fetch and supply multiple instructions during a single memory cycle. The patents-in-suit managed to "break the Von Neumann bottleneck of speed of getting the next instruction," by disclosing a preferred embodiment able to fetch and supply "4 instructions per memory cycle," ('749 patent, 7:12-18; Mar Dec., Ex. M) over prior art which was capable of fetching and supplying only one

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

instruction at a time. A preferred embodiment teaches instructions of a mere 8 bits, so that over a 32 bit bus, a microprocessor practicing the invention could fetch and supply 4 instructions at once. One way the patent taught to shorten instructions was to employ a push down stack, which "allows the use of implied addresses, rather than the prior art technique of explicit addresses for two sources and a destination." *Id.* at 7:18-22. Using a stack for math and logic instructions pops operands from the stack and pushes the result back onto the stack without requiring addresses. *Id.* at 33:67-34:1.

In addition to implied addressing, the patents further disclose that (a) a stack can be configured as a register file and therefore be made addressable, and (b) instructions that access stack elements by address can be kept short, thereby preserving the benefits of parallel fetch.

The patents clearly and repeatedly teach that a push down stack can be configured as an addressable register file:

> The Return Stack 134 is implemented as 16 on-chip RAM locations…The microprocessor allows these 16 locations to also be used as ***addressable registers***. The 16 locations may be read and written by two instructions which indicate a Return Stack relative address from 0-15.

Id., 31:46-57 (emphasis added). In prosecution the inventors reiterated that a push down stack may be "configured as a register file," and that such an organization "conveys the benefits of both stacks and registers." '749 Pros. Hist.; Mar Dec., Ex. N at TPL0001097; *see also*, '749 patent, 3:13-15; Mar Dec., Ex. M ("The register file desirably is a second push down stack"). It was well known that a register file uses addresses. *See id*. 15: 28-30; fig. 13. Accordingly, one of skill in the art would recognize that under the patents the ALU and push down stack could interact using addresses to specify the location of the top and next registers that provide inputs to, and receive outputs from the ALU, and that these registers could be registers from a register file regardless of whether it is organized from the Return or Parameter stack.

3. Plaintiffs' Construction Of The Related Terms Is Wrong For the Same Reasons.

The related claim terms in dispute similarly recite that the ALU is connected to the push down stack (with variations in detail):

- "ALU having an output connected to said means for storing a top item" (JCCS Row 3) ('749 patent, claims 1 and 9)
- "(a) a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and (b) a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input" (JCCS Row 9) ('749 patent, claim 1)
- "an output of said arithmetic logic unit being connected to said top item register" (JCCS Row 16) ('890 patent, claim 1)
- "push down stack with a top item register and a next item register, connected to provide inputs to the arithmetic logic unit" (JCCS Row 15) ('890 patent, claim 1)

Plaintiffs' proposal to import "directly coupled … such that source and destination addresses are not used" fails for each of these terms for the reasons stated above.

This same issue arises in connection with means-plus-function claim elements[5] that describe the connection of the ALU to the top and next registers of the stack:

(a) "means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input" and

(b) "means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input"

These elements are found in '749 Patent, claims 1 and 9 (JCCS Row 8).

The parties' propose the following constructions:

Plaintiffs' Construction	TPL's Construction
(a) Function: storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input Structure: Top item register 76 of stack 74 **directly coupled** to a first input of ALU 80 through line 82 **such that source and destination addresses are not used.** (b) Function: storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input Structure: Next item register 78 of stack 74 **directly coupled** to a first input of	Function***: Ordinary meaning, unless defined elsewhere, including "arithmetic logic unit" and "connected to"*** Structure***: register or its equivalents***

[5] In construing a means-plus-function claim, the court must first determine the claimed function and then identify the corresponding structure that performs that function. *Applied Med. Res. Corp. v. U.S. Surgical Corp.*, 448 F.3d 1324, 1332 (Fed. Cir. 2006).

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

ALU 80 through line 84 **such that source and destination addresses are not used.**	

Plaintiffs' proposed function quotes the claim language, so the parties are essentially in agreement that the claimed function should be understood as its ordinary meaning. TPL adds that sub-terms elsewhere construed should be incorporated into the construction, which should be uncontroversial. The disagreement again is whether the corresponding structure should be limited to elements "directly coupled…such that source and destination addresses" may not be used. As explained above, Plaintiffs' extraneous limitations on the operation of stacks are improper.

TPL properly construes the corresponding structure as a "register or its equivalents." Figure 2 discloses a top item register 76 and a next item register 78, '749 patent, 6:28-35; 19:6-8; Mar Dec., Ex. M (ALU connected to register 76 "by line"). Case law permits a patent owner to prove infringement by pointing to the disclosed structure or its ***equivalents***. *McGinley v. Franklin Sports, Inc.*, 262 F. 3d 1339, 46-48 (Fed. Cir. 2001). Indeed, Figure 21 discloses one such alternative, on-chip latches,[6] as a substitute for the registers. Accordingly, alternatives to registers such as latches are not only permissible as a matter of law but also expressly disclosed, and TPL's construction is correct.

B. <u>"Multiple Sequential Instructions" and Related Terms</u>

1. "Multiple Sequential Instructions" (JCCS Row 7)

The broad claim term "multiple sequential instructions" is found in both Claims 1 and 9[7] of the '749 Patent, and its construction is closely related to three other claim terms.

Plaintiffs' Construction	TPL's Construction
Two or more instructions in sequence, **in which any operand that is present must be right-justified in the instruction register**	Two or more instructions in ***a program*** sequence

TPL's proposed construction of this term is very similar to the first half of Plaintiffs' proposed construction, but Plaintiffs add the limitation "in which any operand that is present must

[6] These are "the fastest form of memory device built on the chip, delivering data in as little as 3 n[ano]s[econds]." *Id.* at 19:13-15.

[7] The '749 patent has been in reexamination since March 2008, and Claims 1 and 9 are currently pending in that reexamination.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

be right-justified in the instruction register." JCSS Row 7. Defendants' construction follows the guidance of *Phillips v. AWH Corp*., 415 F.3d 1303 at 1312, where the words used in a claim are generally given their ordinary and customary meaning. Here, "multiple" means "two or more," and "sequential instructions" means "instructions in a program sequence." Plaintiffs' proposal goes beyond the claimed sequential instructions in an attempt to sweep in instruction registers themselves, and operands within those registers. This is wrong.

Plaintiffs erroneously seek to limit the claim to variable width operands, but variable width operands are only a preferred embodiment in the specification, and should not be read into the claims when the claim language is broader than the embodiments, as is the case here. *See Electro Med. Sys., S.A. v. Cooper Life Sci., Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994). Although variable width operands must be right-justified in the instruction register (*see* '749 patent, 18:33-45; Mar Decl., Ex. M), not all operands in the '749 patent are variable width, nor must they all be right-justified in the instruction register. As but one example, the specification describes 8 bit instructions that consist of a 4-bit opcode and a 4-bit operand. *Id*., 31:35-32:16. Such 8-bit instructions can be located anywhere in the instruction register, and thus the corresponding operand is not necessarily right-justified in the instruction register. Because Plaintiffs' construction would read out these preferred embodiments, it should be rejected.[8]

2. "Sequence of program instructions" (JCCS Row 30)

This claim term is found in Claim 4 of the '148 patent. Defendants propose it be construed simply as "one or more instructions in a program sequence." Plaintiffs once again seek

[8] The prosecution history contains a 10/25/94 Examiner Interview Summary, where the examiner's handwritten notes say "Claim 1: Opera. Width is variable & right adjusted." Mar Decl., Ex. O at TPL0001136. In the Response to Office Action leading up to that interview, the applicants were overcoming the Boufarah prior art reference. In the amendment filed immediately after the interview, the applicants acknowledged a possible amendment to add variable width operands to overcome Boufarah, but never entered that claim language. '749 Pros. Hist.; Mar Dec., Ex. W at TPL0001169-1171. It is a "bedrock principle" that "the claims of a patent define the invention" and "we look to the words of the claims themselves." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576 (Fed.Cir.1996). An unadopted amendment accordingly cannot limit the claims. Similarly, the unadopted amendment "does not show any clear and unambiguous disavowal" of claim scope. *Invitrogen Corp. v. Biocrest Mfg.*, L.P., 327 F.3d 1364, 1369 (Fed. Cir. 2003).

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

to import the restriction "in which any operand that is present must be right-justified in the instruction register. *See* JCCS Row 30. Without that improper limitation, as discussed above, Plaintiffs' proposed construction is "two or more instructions in sequence." Since a sequence of instructions can be one or more, the Court should adopt Defendants' proposed construction.

3. "Instruction register" (JCCS Row 12)

This term is found in Claim 1 of the '890 patent. The parties agree on the construction "register that receives and holds one or more instructions for supplying to circuits that interpret the instruction," JCCS Row 12, but Plaintiffs seek to import the same restriction as noted above. For the reasons previously discussed, the Court should adopt Defendants' construction.

4. "Supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" (JCCS Row 5)

This term is found in Claim 1 of the '749 patent. Plaintiffs' proposed construction differs from Defendants' in that Plaintiffs seek to add limitations indicated by the bolded language:

Plaintiffs' Construction	TPL's Construction
Provide the multiple sequential instructions in parallel **(as opposed to one-by-one)** to said central processing unit integrated circuit during a single memory cycle **without using a prefetch buffer or a one-instruction-wide instruction buffer that supplies one instruction at a time**	Provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle

Once again, Plaintiffs improperly narrow the claim by importing limitations into the plain language of the claim. Indeed, the specification does not *exclude* systems that contain a prefetch buffer, and none of Plaintiffs' intrinsic evidence cited in the JCCS suggests that it does. Rather, the patent teaches the feature of being able to fetch and supply multiple instructions in parallel in a single cycle without *using* an intervening prefetch buffer.

This is supported by the prosecution history. The inventors overcame a rejection for anticipation by the Transputer references, Edwards and May. While the Transputer references disclosed fetching instructions into a prefetch buffer, the instructions were not supplied to the instruction register until a second memory cycle, thus distinguishing them from the '749 patent. The inventors traversed the rejection by noting that "[f]etching multiple instructions into a

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation -- the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'" '749 Reexam Hist.; Mar Decl., Ex. Q at TPL0554266. That does not mean that using a prefetch buffer to fetch multiple instructions is not within the claim; the key is to have the instructions supplied in a single memory cycle. While Edwards (May) disclosed a memory controller that fetched multiple instructions, it supplied them only one at a time, and therefore did not meet the claim.[9] Plaintiffs' attempt to narrow the claim fails, and the Court should adopt Defendants' constructions.

C. "Main CPU" and "Separate DMA CPU"

Main CPU, and the related claim term, "separate DMA CPU," are found in Claim 1 of the '890 patent, and should be construed consistently.

1. Main CPU (JCCS Row 11)

Plaintiffs' Construction	TPL's Construction
Main CPU that does not perform direct memory access related operations	***A main electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions***

Defendants propose the ordinary meaning of "Main CPU," and this construction has the benefit of being nearly identical to Judge Ward's Order construing CPU as found in the '336 patent in the Texas litigation[10] (*see* Mem. Op. and Order, June 15, 2007, 9 ("Ward Order"; Mar Decl., Ex. A) ("an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions").

The construction is also supported by the specification, dictionary definitions, and prosecution history. In the March 27, 2009 Response to the Office Action in the reexamination of

[9] May discloses parallel register banks, but because it has only one instruction buffer which holds only one instruction, all instructions must pass through that single buffer, and only one instruction at a time is supplied to the CPU. '749 Reexam Hist.; Mar Dec., Ex. R at TPL-VO007138.

[10] TPL previously litigated infringement of the '336 and '148 patents, which are at issue in this case, in *TPL v. Fujitsu Ltd., et al.*, Case No. 2:05-CV-00494 (E.D. Tex.). Judge Ward's Order in the Texas litigation construed several claim terms that are identical or related to the claim terms in dispute in this case.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

the '148 patent, Applicants pointed out that "[t]he processing unit operating in accordance with a predefined sequence of program instructions requires a device configured to execute the program instructions. . . .[T]he specification shows that the broadest reasonable interpretation consistent with the specification of the recited processing unit is a device configured to execute the predefined sequence of program instructions. Col. 4, ll. 1-3" (further citations omitted). Mar Decl., Ex. J at TPL0545737-38. *See also,* Computer Dictionary (1991)(CPU is "the device that interprets and executes instructions"); American Heritage Dictionary (1985)(CPU is "[t]he part of a computer that interprets and executes instructions.") Mar Decl., Exs. T and U.

Plaintiffs attempt to narrow the ordinary meaning of CPU by limiting it to "not performing direct memory access related operations," but Plaintiffs are wrong, as their expert Dr. Wolfe testified that the main CPU can initiate memory transfers.[11] As this falls within the realm of "direct memory access related operations," even Plaintiffs' expert appears to disagree with Plaintiffs' proposal. The Court should adopt TPL's construction.

2. Separate DMA CPU (JCCS Row 14)

Plaintiffs' Construction	TPL's Construction
a separate CPU that fetches and executes instructions for performing direct memory access without using the main CPU	***Electrical circuit for reading and writing to memory that is separate from a main CPU***

Claim 1 of the '890 patent claims:

> A microprocessor, which comprises a main central processing unit and a *separate direct memory access central processing unit* in a single integrated circuit comprising said microprocessor, ... said *direct memory access central processing unit* providing inputs to said memory controller ....

'890 patent, 32:44-47, 64-65; Mar Dec., Ex. K (emphasis added). Plaintiffs do not offer a definition of the claimed terms. Instead they restate the term with additional limitations that are not supported by the specification, in this case excluding the element "direct memory access" ("DMA") from use of the main CPU. Yet the claim language includes no such prohibition, nor is there support for that limitation in the specification. In contrast, Defendants' construction is

[11] (Q. [Can the main CPU in the '890 patent] [i]nitiate a transfer or request for data from memory? A. Well, it certainly can request a single element of data from memory, that's one of its capabilities, yeah.") Wolfe Dep. 167:19-168:10; Mar Dec., Ex. V.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

correct because it describes the "DMA CPU" as properly distinct ("separate") from the main CPU, in keeping with the claim structure, and defines the DMA CPU in accordance with the specification, as an "electrical circuit for reading and writing to memory."

The specification includes at least two preferred embodiments of the DMA CPU. The first is shown in Figure 2, where the microprocessor, 50, has a separate DMA CPU, 72, with "the ability to fetch and execute instructions." '749 patent, 8:22-23; Mar Dec., Ex. M. "[A] second embodiment of a microprocessor in accordance with the invention," shown in Figure 9, discloses a DRAM die with on-chip memory and a "DMA CPU" 314. *Id.*, 4:61-62. Here, "the DMA processor 72 of the microprocessor 50 has been replaced with a ***more traditional*** DMA controller." *Id.*, 12:63-65 (emphasis added). This "more traditional DMA controller" is one that functions more as a traditional state machine, without the ability to fetch its own instructions that characterizes a CPU. *See, e.g., id.*, 1:55-58, Background of the Invention (DMA controllers in conventional microprocessors "can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required."). As the specification discloses at least two embodiments of a DMA CPU and Plaintiffs' construction would exclude the "traditional" "DMA CPU 314" of Figure 9, it is incorrect.

D. "Connected to" (JCCS Row 10, '749 patent, *passim*)

TPL construes "connected to" as "connected to convey signals to." Plaintiffs construe this term to include a "directly coupled" limitation for some terms and leave the door open for other undisclosed constructions of this term depending on how various components interact elsewhere:

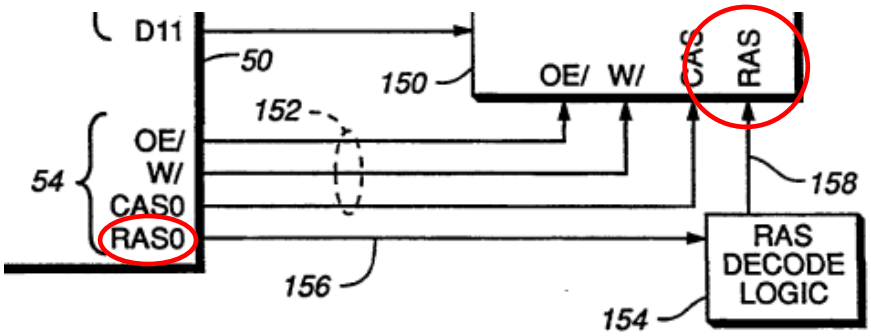
Plaintiffs' Construction	TPL's Construction
In 6.1 and 27.1, [sic] "connected to" means "**directly coupled . . . such that source and destination addresses are not used;" in other contexts, the meaning of "connected to" depends upon how the connected components are supposed to interact.**	***Connected to convey signals to***

TPL's construction is correct and supported by the specification. Plaintiffs' attempt to substitute the term "directly coupled" for "connected to" in various claim terms is misplaced because throughout the specification, two components can be connected to convey signals without being

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

directly connected.[12]

Figure 3 illustrates that components on an integrated circuit can be considered connected despite intervening circuit elements.



In this embodiment, "row address strobe 54 is ***connected through row address strobe decode logic 154 to*** the row address strobe input of the DRAM by lines 156 and 158." '749 patent, 7:40-43; Mar Dec., Ex. M. As the two circled elements here are "connected" through another logic element (154) the term "connected to" as used in the specification permits for the presence of intervening structures.[13] If "connected to" required "direct coupling" or required a connection "without any intervening structure" then the claims would not read on this preferred embodiment. Such constructions are rarely, if ever, correct.[14] *See Chimie*, 402 F.3d at 1377.

[12] Plaintiffs' construction attempts to again import the erroneous limitations prohibiting the use of source and destination addresses. This is discussed above in construction of Push Down Stacks. *See* Section IV (A2).

[13] Plaintiffs' expert, Dr. Wolfe, concedes that connected items could have at least buffers and switches in their path, wholly undercutting Plaintiffs cramped construction. Wolfe Dep. 79:25-80:7; Mar Dec. Ex., V ("Certainly, having a ***buffer*** along the way to repower the signal, I think they would still be connected. I think that possibly even you could have a ***switch*** along the way. I don't think it's that limiting" (emphasis added).

[14] Plaintiffs' construction is also improper and wholly unworkable because it varies in an undisclosed manner "depend[ing] upon how the connected components are supposed to interact." JCCS Row 10.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

E. "Ring Oscillator" and Related Terms (JCCS Row 22)

1. "Ring Oscillator" was Correctly Construed by Judge Ward

Plaintiffs' Construction	TPL's Construction
An oscillator having a multiple, odd number of inversions arranged in a loop, **wherein the oscillator is: (1) non-controllable; and (2) variable based on the environment**	An oscillator having a multiple, odd number of inversions arranged in a loop

"Ring oscillator" is found in claims 1, 11, and 15 of the '336 patent, in claim 7 of the '890 patent, and in claims 4 and 11 of the '148 patent. The parties agree that a ring oscillator is "[a]n oscillator having a multiple, odd number of inversions arranged in a loop…" This was Judge Ward's claim construction and accords with the full and ordinary meaning of the term. Plaintiffs propose additional limitations, including that the oscillator be (1) non-controllable, and (2) variable based on the environment, but they are wrong.

The specifications set forth that ring oscillators are controllable, at a minimum, by temperature and voltage. '336 patent, 16:59-60; Mar Dec., Ex. B ("The ring oscillator frequency is determined by the parameters of temperature, voltage and process").

Plaintiffs' additional proposed limitation of "variable based on the environment" is ambiguous since "the environment" is not clearly defined. According to the '336 specification, "the ring oscillator frequency is determined by the parameters of temperature, voltage, and process." *Id.*, 16:59-60. This is the only "environment" that is disclosed in the specification.[15]

2. Judge Ward properly found a limited disclaimer of systems that ***directly*** rely on an external ***command input*** control signal or crystal / clock to ***generate*** a clock signal.

In the remaining three terms relating to ring oscillators, Plaintiffs have not only tacked on improper limitations to the ring oscillator, as described above, but they also do not acknowledge that the patents exclude only those clocks that ***directly rely*** on an external clock or ***command input*** control signal ***to generate*** a clock signal. The three terms, and the parties' proposed constructions, are as follows:

[15] The same arguments apply to the claim term "ring oscillator variable speed system clock connected to said main central processing unit" (JCCS Row 13 '890 patent, claim 7), where the parties agree on the term's construction but for the addition of Plaintiffs' improper limitations.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

a. "an entire oscillator disposed upon said integrated circuit substrate" (JCCS Row 19) ('336 patent, claims 6 and 13)

Plaintiffs' Construction	TPL's Construction
An oscillator that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal, **wherein the oscillator is: (1) non-controllable; and (2) variable based on the environment**	An oscillator that is located entirely on the same semiconductor substrate as the CPU and does not ***directly*** rely on a ***command input*** control signal or an external crystal/clock generator to generate a clock signal

b. "an entire ring oscillator variable speed system clock in said single integrated circuit" (JCCS Row 23) ('336 patent, claims 1, 11)

Plaintiffs' Construction	TPL's Construction
A ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal, **wherein the ring oscillator variable speed system clock is: (1) non-controllable; and (2) variable based on the environment**	A ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not ***directly*** rely on a ***command input*** control signal or an external crystal/clock generator to generate a clock signal

c. "providing an entire variable speed clock disposed upon said integrated circuit substrate" (JCCS Row 28) ('336 patent, claims 10 and 16)

Plaintiffs' Construction	TPL's Construction
providing a variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal, **wherein the ring oscillator variable speed system clock is: (1) non-controllable; and (2) variable based on the environment**	providing a variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not ***directly*** rely on a ***command input*** control signal or an external crystal/clock generator to generate a clock signal

TPL's construction comes directly from Judge Ward's claim construction of "an entire ring oscillator variable speed system clock in said integrated circuit." Ward Order, 11-12; Mar Dec. Ex. A. Judge Ward determined that the prior art the patent owner overcame to gain allowance disclosed direct reliance on an external crystal clock signal or command input to generate a clock signal. *See* '336 Pros. Hist.; Mar Dec., Ex. C at TPL0001905 (invention

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

"contemplates providing a ring oscillator clock and microprocessor within the same integrated circuit" rather than prior art's "provision of frequency control information to an external clock."); '336 Pros. Hist.; Mar Dec., Ex. D at TPL0001920 (arguing "[i]n Sheets [prior art], a command input is required to change the clock speed."); '336 Pros. Hist.; Mar Dec., Ex. E at TPL0001931 (Magar prior art uses a "conventional crystal clock."). Judge Ward construed the disclaimer in light of these references to mean "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not ***directly rely*** on a ***command input control signal*** or an ***external crystal/clock generator*** to generate a clock signal." Ward Order, 12; Mar Dec. Ex. A (emphasis added). Notably Judge Ward declined the Defendants' invitation to exclude any use of an external clock as a reference signal. Critically, Plaintiffs' ignore the fact the prior art cited by Judge Ward lacked the on-chip oscillator feature of the '336 patent. Plaintiffs' attempt to broaden the disclaimer by modifying Judge Ward's construction should be rejected.

F. "Operates asynchronously to" and Related Terms (JCCS Row 29)

The claim term is found in claims 11, 13 and 16 of the '336 patent, and the parties' competing constructions are as follows:

Plaintiffs' Construction	TPL's Construction
operates without a timing relationship to/with	***timed by independent clock signals***

The '336 patent and its "dual clock" innovation support TPL's construction. The specification section entitled "ASYNCHRONOUS / SYNCHRONOUS CPU" describes "a dual clock scheme as shown in FIG. 17, with the CPU 70 operating asynchronously to I/O interface." '336 Reexam Cert., 1:21-23; Mar Dec., Ex H. The basis of the asynchronous operation of the CPU and I/O interface is that the two devices are timed by two independent clock signals. Figure 17 shows two independent clocks timing the CPU and I/O interface, and claim 11 recites:

> an entire ring oscillator variable speed system clock … connected to said [CPU] . . . and a second clock ***independent*** of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit ***operates asynchronously to*** said input/output interface.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

'336 Reexam Cert., 3:8-11, 22-26; Mar Dec., Ex. H. The specification further discloses "a ring counter variable speed system clock connected to the central processing unit" and a "second clock ***independent*** of the ring counter variable speed system clock [] connected to the input/output interface." '336 patent, 3:27-28, 23-24; Mar Dec., Ex. B.

The applicants introduced "asynchronously" during prosecution "in order to clarify the meaning of 'independent' as recited in the claims." '336 Reexam Hist.; Mar Dec. Ex. G at TPL0549470-71. They cited a treatise to the USPTO that explained, "[a]n asynchronous system is one containing two or more independent clock signals." '336 Reexam Hist.; Mar Dec. Ex. F at TPL0553776. The applicants further argued "that an asynchronous system is effectively a collection of *independent* synchronous systems…" *Id.* Plaintiffs' expert Dr. Wolfe agreed that asynchronous and independent "mean[] pretty much the same thing." Wolfe Dep., 134:8-11; Mar Dec. Ex. V. In light of this evidence, "timed by independent clock signals" properly captures the meaning of "operates asynchronously to" in the claims of the '336 patent.[16]

For the remaining related terms, the parties dispute whether the second clock signal and the ring oscillator are "initially generated" or merely "generated" by a different source:

- "a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock" (JCCS Row 25) ('336 patent, claim 1)

Plaintiffs' Construction	TPL's Construction
a clock signal of said second clock is **initially generated** by a different source than said ring oscillator variable speed system clock	a clock signal of said second clock is ***generated*** by a different source than said ring oscillator variable speed system clock

- "a clock signal from said off-chip external clock originates from a source other than said oscillator" (JCCS Row 26) ('336 patent, claim 6)

Plaintiffs' Construction	TPL's Construction
a clock signal from said off-chip external clock is **initially generated** by a different source than said oscillator	a clock signal of said off-chip external clock is ***generated*** by a different source than said oscillator

[16] *See also*, '336 Reexam Hist.; Mar Dec., Ex. F at TPL0553771-785; Ex. G at TPL0549461-462, TPL0549464, TPL0549467-473 and the US'336 Reexamination Certificate, col. 1 (replacing col. 17, ll. 12-37); Mar Dec., Ex. H at TPL0548763.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

- "a clock signal from said off-chip external clock originates from a source other than said variable speed clock" (JCCS Row 27) ('336 patent, claim 10)

Plaintiffs' Construction	TPL's Construction
a clock signal from said off-chip external clock is **initially generated** by a different source than said variable speed clock	a clock signal of said off-chip external clock is ***generated*** by a different source than said variable speed clock

TPL's proposed construction, requiring the second clock, external clock, and off-chip clock to be "generated" by a different source than the variable speed clock, accords with the patent's premise that the ring oscillator clock and second clock be "independent." Judge Ward construed "system clock" and "variable speed clock" as "a circuit that ***generates*** the signal(s) used for timing the operation of the CPU." Ward Order, 13; Mar Dec., Ex. A. Plaintiffs agreed to this construction. JCCS Ex. A, Row 27. It follows then that the clock signal for the second clock, which the patent teaches is "independent," should be "***generated*** by a different source than said variable speed clock," as TPL proposes (and as multiple reexaminations of the '336 patent have confirmed). Plaintiffs' phrase "initially generated" comes out of nowhere, and has no support in the intrinsic evidence. In contrast, TPL's construction properly tracks Judge Ward's order, the lessons of the multiple reexaminations, captures the independence of the two clocks, and is supported by the specification.

V. MEANS PLUS FUNCTION CLAIMS OF THE '749 PATENT

The '749 patent contains several means plus function claims, reading on the multiple instruction fetch, multiplexing and push down stack optimization features of the invention. 35 U.S.C. § 112, ¶6 of the Patent Act permits claiming in a "means plus function" form; in construing a means-plus-function claim, the court must first determine the claimed function and then identify the corresponding structure that performs that function. *Applied Med. Res. Corp. v. U.S. Surgical Corp.*, 448 F.3d 1324, 1332 (Fed. Cir. 2006).

A. "means connected to said bus for fetching instructions" (Row 4) ('749 patent, claim 1)

Plaintiffs' Construction	TPL's Construction
Function: fetching instructions for said central processing unit integrated circuit on said bus from said memory, being	Function: fetching instructions for said central processing unit integrated circuit on said bus from said memory, being

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle Corresponding §112 ¶6 structure (Fig. 4): Memory controller 118 **connected to** instruction register 108 **through** internal data bus 90 **and, to** program counter 130 **through** internal address bus 136, **and to Request Instruction Fetch-Ahead 192 via line 196, and Request Instruction Fetch-Ahead 192 is connected to instruction register 108 via lines 194.**	configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle, ***wherein the fetched "multiple sequential instructions" are supplied to the instruction register 108 during the same memory cycle they are fetched.*** Corresponding §112¶6 structure: Memory controller (118) Instruction register (108) Internal data bus (90) Program counter (130) Internal address bus (136)

1. The claimed function requires the fetching means to supply instructions during the same memory cycle in which it fetches.

Both parties propose the function defined literally in the claim, which reads:

> means connected to said bus for **fetching instructions for said central processing unit integrated circuit on said bus from said memory**, said means for fetching instructions **being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle,**[17]

Claim 1, '749 patent, 35:14-26; Mar Dec., Ex. M (emphasis added). TPL clarifies the "in parallel" and "single memory cycle" aspects of the fetching and supplying function by including the language "wherein the fetched 'multiple sequential instructions' are supplied to the instruction register 108 during the same memory cycle they are fetched."

This multiple instruction fetch and supply feature of the '749 patent was one of its "architectural innovations." *Id.*, 26:16-29. This provided many advantages including "increased

[17] Claim 9 contains a similar but slightly different means plus function element: "means connected to said bus for fetching instructions for said central processing unit on said bus from said dynamic random access memory, said means for fetching instructions being configured to fetch multiple sequential instructions from said dynamic random access memory in parallel and supply the multiple instructions to said central processing unit during a single memory cycle." '749 patent at 37:15-22; Mar Dec., Ex. M.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

execution speed even with slow memories," and "opportunities to optimize groups of instructions." *Id*. This feature overcame "the bottleneck" in most computer systems," as "[t]he ability to fetch four instructions in a single memory bus cycle significantly increases the bus availability to handle data." *Id*., 5:54-58.

TPL's proposed function emphasizes that the parallel fetch brings the instructions from memory to the instruction registers of the CPU in the requisite single memory cycle.

> By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.

Id., 8:13-16. This passage shows that the fetching operation fetches instructions for "loading into the instruction register." *Id.*, 8:10-16.

This is consistent with TPL's arguments to the USPTO in distinguishing the May prior art:

> Thus, [May has] no mechanism to supply instructions to either O REG 57, let alone means for fetching configured to supply multiple sequential instructions to a central processing unit integrated circuit during a single memory cycle as recited in claim 1.

'749 Reexam Hist.; Mar Decl., Ex. P at TPL0554872.[18] Plaintiffs' expert agreed with this point. Wolfe Dep. 147:13-14, 147:23-148:4; Mar Dec. Ex. V ("[claim 1] says to fetch and supply during a single memory cycle….But my recollection is that it is supplied to the instruction register and also to a selection multiplexer [sic] beyond the -- beyond the instruction register, and also to a detection circuit that determines whether or not the multiple sequential instructions can be fetched in a single cycle.")

2. Claim 1's Fetching Means Does Not Include Fetch Ahead Circuitry.

The parties agree that memory controller (118), instruction register (108), internal data bus (90), program counter (130) and internal address bus (136) all perform the claimed function of fetching instructions from the memory to the CPU on the bus. Plaintiffs also seek to include structures 192, 194 and 196, but this expanded structure should be rejected because the identified components do not fetch. Structures 192, 194 and 196 merely determine by decoding whether

[18] The patent owner made similar arguments in the '749 Reexam Hist.; Mar Dec. Ex. Q at TPL0554266.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

certain conditions are met, and if so a fetch is requested ahead of instruction execution, otherwise a fetch is requested once all instructions in the instruction register have executed. '"The output of decoder 192 on line 196 **requests** an instruction **fetch ahead** by memory controller 118 without interference with other accesses." '749 patent; 8:7-9; Mar Dec., Ex. M (emphasis added). Thus, the fetch itself is only performed by memory controller 118:

> While the current instructions in instruction register 108 are executing, the ***memory controller 118 obtains the address of the next set of four instructions from program counter 130 and obtains that set of instructions***.

Id., 8:10-13 (emphasis added). Figure 4 shows the internal data bus 90 and internal address bus 136 that interconnect the memory controller 118, instruction register 108 and program counter 130. These components are properly construed as the corresponding structure for the fetching means.

B. multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide multiplexed row addresses, column addresses and data on said bus from said central processing unit to said dynamic random access memory and to provide data from said dynamic random access memory to said central processing unit (Row 6) ('749 patent, claim 9)

Claim 9 sets forth the function of the "multiplexing means" as providing "multiplexed row addresses, column addresses and data…," (*id*., 37:8-10) and thus requires a common understanding of "multiplexing." TPL's proposed construction adds the requisite definition to "multiplexing," construing the function of the multiplexing means as "providing data, column addresses, row addresses to a bus, wherein row addresses and column addresses and data **can be provided to the bus at different times,**" as shown below:

Plaintiffs' Construction	Defendants' Construction
Function: being connected and configured to provide **multiplexed** row addresses, column addresses and data on said bus from said central processing unit to said dynamic random access memory and to provide data from said dynamic random access memory to said central processing unit Corresponding §112 ¶6 structure (Fig. 12):	Function: providing data, column addresses, row addresses to a bus, wherein row addresses and column addresses and data ***can be provided to the bus at different times.*** Corresponding §112 ¶6 Structure: MUX

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

(1) MUX 378 connected to MUX 382 **through MUXED ADDRESS BUS 380;** (2) MUX 378 connected to the unnumbered MUX between MUX 378 and MUX 382 **via the two unnumbered MUXED ADDRESS BUSES (labeled "A23 – A13" and "A12 – A2," respectively) between MUX 378 and such unnumbered MUX** (3) MUX 382 connected to the unnumbered MUX between MUX 378 and MUX 382 **via the two unnumbered MUXED ADDRESS BUSES (labeled "A23 – A13" and "A12 – A2," respectively) between MUX 382 and such unnumbered MUX**	(382); MUX (378); and MUX in Fig. 12 between 382 and 378

Plaintiffs' construction adds nothing, because it does not define multiplexing, but instead only reuses the claim language in the proposed function. Because the definition of multiplexing is key to the construction of this term, it should not be ignored. Multiplexing refers to the process by which row addresses, column addresses, and data are moved from the CPU to the external memory. The specification discloses in the timing diagram of Figure 11 that different types of information can be placed onto a bus at different times.

Figure 11 shows a DRAM implementation, where the bus transmits row addresses starting at time (10), followed by column addresses at time (11), and finally data, at time (12). Thus Figure 11 demonstrates that multiplexing is a very broad claim term that reaches the capability of transmitting row addresses, column addresses, and data at different times. The preferred embodiment shows the transfer of different types of information at the same time, however, this exact order is not essential for multiplexing. '749 patent, 5:3-4; Mar Dec., Ex. M. TPL confirmed this feature of multiplexing during prosecution. *See* '749 Reexam Hist.; Mar Dec. Ex. Q at TPL0554297-298.

Finally, Plaintiffs' identified structure is overly inclusive, as the three Muxed Address Buses (labeled A32-24, A23-13, and A12-A2 in Figure 12) are not necessary to perform the multiplexing function.

VI. MISCELLANEOUS DISPUTED CLAIM TERMS OF THE '336 PATENT

The '336 patent's dual asynchronous clock innovation claims a ring oscillator clock on the

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

same chip as the CPU, which is timed such that temperature, voltage, process technology and manufacturing variations similarly affect the performance of both devices. Miscellaneous disputed claim terms speak to this clocking innovation:

A. "[including a plurality of electronic devices] correspondingly constructed of the same process technology with corresponding manufacturing variations" (Row 17) ('336 patent, claim 1)

The pertinent portion of claim 1 of the '336 patent reads:

> A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each ***including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations***, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; …

'336 Reexam Cert., 1:59-2:5 Mar Dec., Ex. H.

Plaintiffs' and TPL's constructions of the highlighted claim phrase follow:

Plaintiffs' Construction	TPL's Construction
Correspondingly constructed **by receiving the same semiconductor manufacturing processes** with corresponding manufacturing variations	Constructed ***using the same manufacturing process technology*** with corresponding manufacturing variations

TPL construes this term to require that the chip be constructed "using the same manufacturing process technology." This refers to the CPU and the on-chip first clock being manufactured on the same substrate such that they are subjected to similar manufacturing variations, and, accordingly, their performance varies similarly.

"Process technology" was introduced during prosecution with an explanation "that operating characteristics of electronic devices in an integrated circuit will track one another depending on variations in the manufacturing process used to make the integrated circuit…." '336 Pros. Hist.; Mar. Decl., Ex. D at TPL0001917, 1919. The specification similarly provides that ring oscillator "performance tracks the parameters which similarly affect all other transistors on the same silicon die." '336 patent at 16:65-67, Mar. Dec., Ex. B.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

The applicant summarized the point to overcome the Magar prior art reference:

> Crucial to the present invention is that ***since both the oscillator or variable speed clock and driven device are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together***. This differs from all cited references in that the oscillator or variable speed clock and the driven device are on the same substrate, and that the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.

'336 Pros. Hist.; Mar. Decl., Ex. E at TPL0001933 (emphasis added). See also *Id*., Ex. C at TPL0001904. Thus, "the process technology" of this claim term refers to the overall fabrication parameters used on the single silicon substrate on which both the CPU and ring oscillator are made. Plaintiffs' construction would go much farther by importing the vague and uncertain limitations of "receiving" and "semiconductor manufacturing processes," neither of which is illuminated by the intrinsic evidence. Defendants' proposed construction should be adopted.

B. <u>"clocking said central processing unit" (JCCS Row 20) ('336 *passim*)</u>

Plaintiffs' Construction	TPL's Construction
Driving said central processing unit **without using any control input or any external clock**, **oscillator** or **crystal such that said central processing unit always executes, the maximum frequency**, **but never too fast**	***timing the operation of the CPU***

The specification describes a ring oscillator variable speed system clock connected to the CPU that times the operation of the CPU. TPL's construction follows Judge Ward's construction for "oscillator . . . clocking," ("an oscillator that generates the signal(s) used for ***timing the operation of the CPU***") Ward Order at 13, and is consistent with the term's ordinary meaning. Plaintiffs' own expert agrees. Wolfe Dep. 135:20-24; Mar Dec. Ex. V ("general ordinary meaning would have been providing an oscillating signal that can be used as a timing reference for the circuits in the central processing unit, basically providing a clock"). Plaintiffs' attempt to narrow this term beyond its ordinary meaning is improper.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

C. "exchanging coupling control signals, addresses and data" (JCCS Row 18) ('336 patent, Claims 6 and 10)

This term relates to the interaction between the CPU and the integrated circuit's input / output (I/O) interface. The claim requires:

> an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit….

'336 patent Reexam Cert. 2:5-7; *see also*, Abstract; *see also*, 3:31-33; Mar Dec., Exs. H, B. The competing constructions:

Plaintiffs' Construction	TPL's Construction
Transmitting **and** receiving coupling control signals, addresses, and data	Transmitting ***and/or*** receiving coupling control signals, and addresses, and data

"Exchanging" contemplates that the CPU may transmit ***and/or*** receive the various types of signals. Plaintiffs' contention to the contrary is not supported by the specifications, and would read out the embodiment depicted in Figure 6, where addresses go in only one direction from SH-BOOM to EPROM, and not in reverse. *See id*. at 8:30-32 ("Data lines 52 D9-D18 provide addresses to address terminals 264 of the EPROM 260."). TPL's construction, permitting some data types to be transmitted but not received, thus accords with the specification.

Plaintiffs' construction is also ambiguous. It does not make clear whether all signals must be both transmitted and received, or at least one signal must be both transmitted and received, or at least one signal must be transmitted and at least one signal must be received. Plaintiffs' construction should be rejected.

D. "as a function of parameter variation" (JCCS Row 21) ('336 patent, claim 6)

Plaintiffs' Construction	TPL's Construction
in a **determined functional relationship** with parameter variation	Based on parameter variation

Claim 6 of the reissued '336 patent claims:

> varying the processing frequency of said first plurality of electronic devices [comprising the CPU] and the clock rate of said second plurality of electronic devices [the oscillator clock] in the same way ***as a function of parameter variation*** in one or more fabrication or operational parameters associated with said integrated circuit substrate . . .

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

'336 Reexam Cert., 2:22-28; Mar Dec., Ex. H (emphasis added). This term, read in context, means that as fabrication or operational parameters – such as voltage, temperature and process technology – vary, the CPU frequency and oscillator clock vary too.

Plaintiffs' construction is too restrictive because it requires a "determined ***functional*** relationship." This construction suggests the existence of an algebraic function to predict the CPU frequency and clock rate, even though no such mathematical relationship is disclosed in the specification. Plaintiffs' construction is also confusing because, (a) it construes "function" by relying on the word "functional," which is circular and unhelpful, and (b) it uses the phrase "functional relationship" which the PTO used in a completely different sense during prosecution. *See e.g.*, '336 Pros. Hist.; Mar Dec., Ex. C at TPL0001903 (specifying "functional relationship" as "ring oscillator variable speed system clock is disposed to clock the central processing unit"). Plaintiffs' construction should be rejected.

E. "external clock" (JCCS Row 24) ('336 patent, claims 10, 13 and 16)

Plaintiffs' Construction	TPL's Construction
A clock not on the central processing unit	A clock not on the integrated circuit substrate

TPL's construction is based on Judge Ward's claim construction order construing "external clock" as "a clock not on the integrated circuit substrate." Ward Order, 16; Mar Dec., Ex. A. TPL's construction is also supported by the specification. The patents use the term "external" to denote off-chip devices:

> The microprocessor 50, like any RISC type architecture, is optimized to handle as many operations as possible on-chip for maximum speed. ***External memory*** operations take from 80 nsec. to 220 nsec. compared with ***on-chip memory*** speeds of from 4 nsec. to 30 nsec.

'336 patent, 27:16-20; Mar Dec., Ex. B. Here, "external" is the opposite of "on-chip."[19]

[19] This is further supported by the usage of "external" in the claims. "External" is a spatial word, and the spatial frame of reference of the relevant claims is the integrated circuit substrate itself. Claims 10, 13 and 16 recite a device with a ring oscillator clock "disposed upon" the CPU integrated circuit substrate. They contemplate an "on chip input/output interface, an "off-chip external memory bus" and an "off-chip external clock." As the spatial frame of reference of these claims is the integrated circuit substrate (i.e. the chip), "external clock" must refer to something outside of that spatial frame of reference, i.e. something off chip. Indeed, in prosecution, TPL

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400

Plaintiffs' construction, "a clock not on the central processing unit," is flawed because a CPU is only a logical construct until it is created on an integrated circuit substrate. Therefore it is meaningless to suggest a clock circuit is "not on the CPU." A clock can be placed virtually anywhere on the physical surface of an integrated circuit substrate including within or outside the perimeter of the CPU logic. It is the connections that matter. Plaintiffs' expert agreed "I can't think of any reason right now why I would tie it to the CPU. I mean, that doesn't seem to match what's taught in the patent." Wolfe Dep. 102:10-16; Mar Dec., Ex. V. Defendants' construction is correct and should be adopted.

VII. CONCLUSION

For the foregoing reasons, Defendants request the Court enter an order adopting TPL's proposed claims constructions.

DATED: December 9, 2010

FARELLA BRAUN & MARTEL LLP

I represent that concurrence in the filing of this document has been obtained from each of the other signatories which shall serve in lieu of their signatures on this document.

By: /s/
John L. Cooper

Attorney for Defendants
TECHNOLOGY PROPERTIES LIMITED
and ALLIACENSE LIMITED

KIRBY NOONAN LANCE & HOGE LLP

By: /s/
Charles T. Hoge, Esq.

Attorneys for Defendant
PATRIOT SCIENTIFIC CORP.

introduced the term "'off chip' to clarify 'external'." '336 Reexam Hist.; Mar Dec. Ex. G at TPL0549462.

Farella Braun & Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
Telephone: (415) 954-4400